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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,255	03/21/2001	Shunpei Yamazaki	07977-107002	5578

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EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

NOTIFICATION DATE	DELIVERY MODE
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11/25/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 09/814,255	Applicant(s) YAMAZAKI ET AL.	
	Examiner Ori Nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 20,28-31,33-38,40-45,47-53,55 and 56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20,28-31,33-38,40-45,47-53,55 and 56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 20, 28, 31, 34-35, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh (5,159,416) in view of Hollinger (5,089,434).

Regarding claims 20 and 34, Kudoh teaches in figure 9 and related text a semiconductor device having a thin film transistor the thin film transistor comprising:

a semiconductor layer 12 on an insulating surface 11;

a gate insulating film 13 on and in contact with the semiconductor layer, the gate insulating film 13 defining a first contact hole extending from a first opening (a discontinuous in the gate insulating film) located at a top surface of the gate insulating film (at a level where the top surface of layer 15 is located) to a second opening located at a bottom surface of the gate insulating film, and the semiconductor layer defining a recess having a third opening located at a top surface of the semiconductor layer that is in communication with the second opening, the third opening defining an area that is greater than an area defined by the second opening;

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an anodic oxide film (the oxide layer formed on the sidewall of the gate electrode) on the gate electrode;

an interlayer insulating film 98 on and in contact with the anodic oxide film, the interlayer insulating film defining a second contact hole extending from a fourth opening located at a top surface of the interlayer insulating film to a fifth opening located at a bottom surface of the interlayer insulating film, and the anodic oxide film defining a second recess having a sixth opening located at a top surface of the anodic oxide film that is in communication with the fifth opening, the sixth opening defining an area that is greater than an area defined by the fifth opening such that a portion of the interlayer insulating film extends over a portion of the second recess;

a gate electrode 14 on the gate insulating film 13; and

a source electrode 15, 97 in contact with the semiconductor layer through the contact hole,

wherein the source electrode contains a first layer 15 and a second layer 97, and

wherein the recess is filled with the first layer, and

wherein the first layer is in contact with the gate insulating film.

Kudoh does not teach a portion of the gate insulating film extends over a portion of the recess.

Hollinger teach in figure 2 (see also figure 13D) and related text a portion of the gate insulating film (26 and the bottom part of 62) extends directly over a portion of the recess.

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Note that the gate insulating film comprises layers 26 and the bottom part of 62, because layers 26 and 62 comprise silicon oxide and are thus indistinguishable from each other.

Although Hollinger forms the gate insulating film as layers 26 and the bottom part of 62, these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in product by process claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a portion of the gate insulating film to extend over a portion of the recess in Kudoh's in order to improve the device characteristics by having better control over the electrode layer.

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Regarding claims 28 and 35, Kudoh teaches in figure 9 and related text a semiconductor layer contains crystalline silicon, and a silicon oxide interlayer insulating film.

Regarding claims 31 and 38, Kudoh teaches a second layer contains aluminum.

Claims 20, 28, 31, 34-35, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollinger (5,089,434) in view of Kudoh (5,159,416).

Regarding claims 20 and 34, Hollinger teaches in figures 1 and 13D and related text a semiconductor device having a transistor the transistor comprising:

- a semiconductor layer 20;

- a gate insulating film 26, 62 on and in contact with the semiconductor layer, the gate insulating film defining a first contact hole extending from a first opening located at a top surface of the gate insulating film to a second opening located at a bottom surface of the gate insulating film, and the semiconductor layer defining a recess having a third opening located at a top surface of the semiconductor layer that is in communication with the second opening, the third opening defining an area that is greater than an area defined by the second opening such that a portion of the gate insulating film extends directly over a portion of the recess;

- an anodic oxide film (top part of layer 62) on the gate electrode;

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a second insulating film (the other one of 26, 62) on and in contact with the anodic oxide film, the second insulating film defining a second contact hole extending from a fourth opening located at a top surface of the second insulating film to a fifth opening located at a bottom surface of the second insulating film, and the anodic oxide film defining a second recess having a sixth opening located at a top surface of the anodic oxide film that is in communication with the fifth opening, the sixth opening defining an area that is greater than an area defined by the fifth opening such that a portion of the second insulating film extends over a portion of the second recess;

a gate electrode 12a on the gate insulating film; and

a source electrode 16 in contact with the semiconductor layer through the contact hole,

wherein the source electrode contains a first layer 16, and

wherein the recess is filled with the first layer, and

wherein the first layer is in contact with the gate insulating film.

Note that the gate insulating film comprises layers 26 and the bottom part of 62, because layers 26 and 62 comprise silicon oxide and are thus indistinguishable from each other.

Although Hollinger forms the gate insulating film as layers 26 and the bottom part of 62, these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ

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685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in product by process claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Hollinger does not teach using the device as a thin film transistor, such that the semiconductor layer is on an insulating surface, an interlayer insulating film and a source electrode contains a second layer.

Kudoh teaches in figure 9 and related text using the device as a thin film transistor, such that the semiconductor layer is on an insulating surface, an interlayer insulating film and a source electrode contains a second layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Hollinger's device as a thin film transistor, such that the semiconductor layer is on an insulating surface, to use an interlayer insulating film and a source electrode contains a second layer, in order to use the device in an application which requires TFT, to provide better protection to the device, and to improve the contact resistance of the device, respectively.

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Regarding claims 28 and 35, Kudoh teaches in figure 9 and related text a semiconductor layer contains crystalline silicon, and a silicon oxide interlayer insulating film.

Regarding claims 31 and 38, Kudoh teaches a second layer contains aluminum.

Claims 29 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh and Hollinger in view of Aratani et al. (5,854,139).

Kudoh and Hollinger teach substantially the entire claimed structure, as applied to claims 20 and 34 above, except a first layer contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

Aratani et al. teach a source electrode comprising indium silicide (column 8, line 64 to column 9, line 1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Kudoh and Hollinger's silicide layer of indium silicide, in order to improve the characteristics of the device. Note that substitution of materials is not patentable even when the substitution is new and useful. *Safetran Systems Corp. v. Federal Sign & Signal Corp.* (DC NIII, 1981) 215 USPQ 979.

Claims 33 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh and Hollinger in view of Applicant Admitted Prior Art (AAPA).

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Regarding claims 33 and 40, Kudoh and Hollinger teach substantially the entire claimed structure, as applied to claims 20, 34 above, except using the device as an active matrix type EL display device.

AAPA teaches using thin film device as an active matrix type EL display device.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Kudoh and Hollinger's device as an active matrix type EL display device, in order to use the device in an application which requires an active matrix type EL display device.

Claims 30 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh and Hollinger in view of Tanaka et al. (5,798,744).

Kudoh and Hollinger teach substantially the entire claimed structure, as applied to claims 20, 34 above, except a first layer is an alloy of aluminum and germanium.

Tanaka et al. teach a first layer can be silicide or germanium compound (column 9, lines 56-61).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first layer comprises germanium compound instead of silicide in Kudoh and Hollinger's device, in order to improve the device characteristics.

Note that forming a first layer comprises germanium, as taught by Tanaka et al., and a second layer of aluminum, as taught by Kudoh mean that the first layer would comprise aluminum-germanium, because the aluminum would react with the germanium.

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Note that substitution of materials is not patentable even when the substitution is new and useful. *Safetran Systems Corp. v. Federal Sign & Signal Corp.* (DC NIII, 1981) 215 USPQ 979.

Claims 41-45, 47, 49-53 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh in view of Miyakawa (5,278,449).

Regarding claims 41 and 49, Kudoh teaches in figure 9 and related text a semiconductor device having a thin film transistor the thin film transistor comprising:

- a semiconductor layer 12 on an insulating surface 11, wherein the semiconductor layer has a side recess (the area where layer 15 is located);

- a gate electrode 14 adjacent to the semiconductor layer with a gate insulating film 13 interposed there-between, wherein the gate electrode has a second side recess and a wiring 17 in contact with the gate electrode; and

- an interlayer insulating film 98 comprising silicon oxide over at least the gate electrode; and

- a source electrode 15, 97 over the interlayer insulating film, wherein the source electrode is in contact with the semiconductor layer through a contact hole opened in the interlayer insulating film 98, wherein the source electrode contains a first layer 15 and a second layer 97;

- wherein a part of the first layer and a part of the third layer are located directly over the interlayer insulating film,

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wherein the wiring contains a third layer 17 and the fourth layer (the wiring connected to layer 125, see figures 11A and 11B),

wherein the side recess is filled with the first layer 15, and

wherein the second side recess is filled with the third layer, and

wherein the first layer 15 is in contact with the gate insulating film 13.

Kudoh does not teach a part of the second and fourth layers located directly over the interlayer insulating film. That is, Kudoh does not teach forming the first layer as a lamination of two layers, such that part of the second and fourth layers are located directly over the interlayer insulating film.

Miyakawa teaches in figure 7 and related text forming the first layer as a lamination of two layers Ti/TiN.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the first layer as a lamination of two layers in Kudoh's device, such that part of the second and fourth layers are located directly over the interlayer insulating film, in order to improve the device characteristics by using barrier layers, as is well known in the art.

Regarding claims 43, 51 and 44, 52, Miyakawa teaches at least a first layer 151a contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony, and an alloy of aluminum and germanium, respectively.

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It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a first layer contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony, and an alloy of aluminum and germanium, respectively, in Kudoh's device, in order to improve the characteristics of the device. Note that substitution of materials is not patentable even when the substitution is new and useful. *Safetran Systems Corp. v. Federal Sign & Signal Corp.* (DC NIII, 1981) 215 USPQ 979.

Regarding claims 42, 47, 50 and 55, Kudoh teaches in figure 9 and related text a semiconductor layer contains crystalline silicon, and a silicon oxide interlayer insulating film.

Regarding claims 45 and 53, Kudoh teaches a second layer contains aluminum.

Claims 48 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh and Miyakawa in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 48 and 56, Kudoh and Miyakawa teach substantially the entire claimed structure, as applied to claims 41 and 49 above, except using the device as an active matrix type EL display device.

AAPA teaches using thin film device as an active matrix type EL display device.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Kudoh and Miyakawa's device as an active matrix type EL

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display device, in order to use the device in an application which requires an active matrix type EL display device.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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